ISP Core

Datasheet

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1.0 Overview

MRA Digital Sensor Image Processing ISP core provides an easy interface between the Camera Sensor and the display device. The core receives the Raw pixel data from the sensor chip in Bayer Pattern, performs interpolation and converts into RGB format. The RGB data undergoes several stages of image processing before being sent to the display device. The ISP core introduces only few lines of latency in its image processing pipeline. An optional Frame Buffer can also be inserted in the pipeline if frame rate conversion is desired.

The main features of ISP core include:

- Configurable color depth (8/10/12-bit per color).
- Supports up to 1080p60 (1920x1080@60fps) video resolution. Support for higher/custom resolution also available (please contact MRA technical support).
- Supports Bayer pattern and RGB input formats. MIPI input interface is currently under development (contact MRA for further details).
- Output is available in RGB and YCbCr format (optional).
- Configuration registers are accessible through Avalon interface.
- Seamless integration in Altera Qsys system.
- Digitally processes and enhances the quality of an input video stream and collects video statistics data for use in video control algorithms, i.e. Auto White Balance (AWB) and Auto Exposure (AE). Complete and configurable ISP pipeline includes:
  - Defective Pixel Correction
  - Color Filter Array Interpolation (Demosaic)
  - Image Statistics (+ AWB & AE Support)
  - Color Correction Matrix
  - Black level offset correction
  - Saturation Adjustment
  - Gamma Corrections
  - Image Enhancement
  - Motion Adaptive Noise Reduction
  - RGB to YCbCr Color-Space Conversion

2.0 Device Support

The ISP core can be easily implemented on all Altera FPGAs.

- Altera MAX10 FPGAs
- Altera Cyclone FPGAs (III/IV/V)
- Altera Aria FPGAs (V/10)
- Altera Stratix FPGAs (IV /V/10)

3.0 Tool Support

Altera Quartus 13.1 & Higher

4.0 Resource Estimate

Table 1 shows the FPGA resource estimate for the ISP core on Cyclone III device with a color depth of 8 bits and 1920x1080 resolution. The resource consumption is expected to be similar on other Altera devices. The Memory Bits overall usage can vary significantly for different color depths and resolutions. Please contact MRA if resource estimate is needed for any particular resolution and color depth.

FPGA Device	Color Depth	Image Resolution	Logic Cells	Dedicated Logic Registers	Memory Bits	M9Ks	DSP Elements
Cyclone III	8	1920x1080	9335	4955	161858	23	42

Table 1: Resources Usage for Cyclone 3 FPGA

5.0 Performance

The ISP core can be implemented to run up to 150 MHz clock frequency.

6.0 Block Diagram

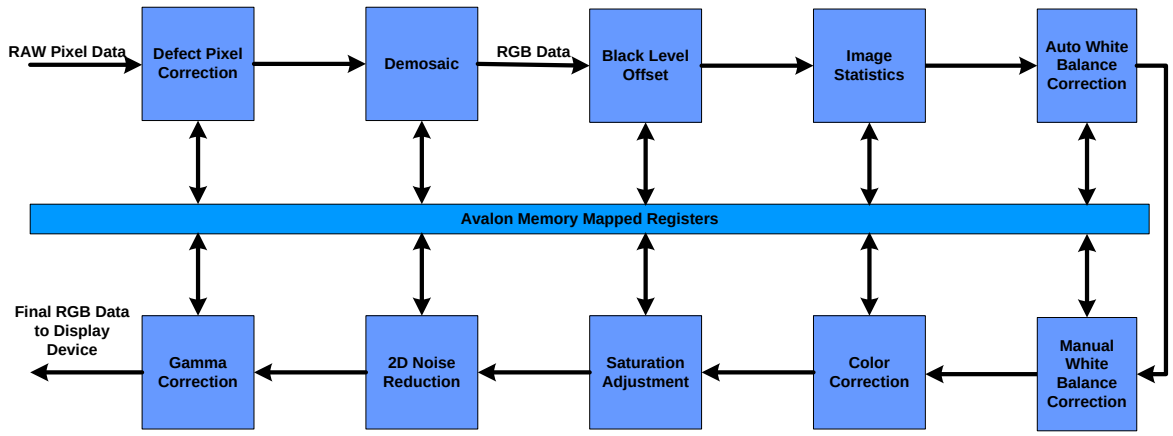

Figure 1: ISP IP Core Block Diagram

7.0 Compile-Time Parameters

Parameter	Type	Valid Values	Default Value	Description
pDATAWIDTH	Integer	8,10,12	8	Bit-width of each color component Red, Green and Blue. The Block RAM and logic cells consumption increases with greater color depth.
pLINE_SIZE	Integer	<= 2048	1920	Maximum horizontal resolution of the input video. The Block RAM and logic cells consumption increases with Line Size.

Table 2: ISP Core Compile-time parameters

8.0 Input / Output Signals

Signal Name	Bit Width	I/O	Description
Input Camera Interface			
iSENSOR_CLK	1	I	Sensor clock from the sensor chip or FPGA PLL output. Data is latched at the rising edge of the clock.
iSENSOR_VSYNC	1	I	VSYNC signal. Start of frame indicator.
iSENSOR_HSYNC	1	I	HSYNC signal. The ISP core can work without this signal. The output HSYNC signal from the ISP core is just the delayed version of this input signal.
iSENSOR_DE	1	I	DE data enable signal. Indicates active video.
iSENSOR_DATA	[pDATAWIDTH-1:0]	I	RAW data in Bayer pattern from the Sensor chip. pDATAWIDTH = {8,10,12}
Video Output Interface (Synchronized with iSENSOR_CLK)			
oVIDOUT_VSYNC	1	O	Vertical blanking VSYNC signal.
oVIDOUT_HSYNC	1	O	Horizontal blanking HSYNC signal.
oVIDOUT_DE	1	O	DE signal. Indicates active video.
oVIDOUT_RED	[pDATAWIDTH-1:0]	O	Video Red data.
oVIDOUT_GREEN	[pDATAWIDTH-1:0]	O	Video Green data.
oVIDOUT_BLUE	[pDATAWIDTH-	O	Video Blue data.

	1:0]		
Configuration Avalon Interface			
iAV_CLK	1	I	Avalon clock.
iAV_RESET	1	I	Avalon Reset.
iAV_ADDRESS	[13:0]	I	Avalon Address.
iAV_READ	1	I	Avalon Read.
iAV_WRITE	1	I	Avalon Read.
iAV_BYTEENABLE	[3:0]	I	Avalon Byte Enable.
iAV_WRITEDATA	[31:0]	I	Avalon Write Data.
oAV_READDATA	[31:0]	O	Avalon Read Data.
oAV_READDATA_VALID	1	O	Avalon Read Data Valid.
oAV_WAITREQUEST	1	O	Avalon Wait Request.

Table 3: ISP Core Input / Output Signals

9.0 Applications

The ISP IP cores enables developers of video surveillance, medical imaging, defense application to create advanced video products and applications low with risk, and with faster time to market. In addition, when used with our ready-made hardware platforms, the complexity of developing and deploying high performance custom video/imaging products is now reduced to just placing an order with us.

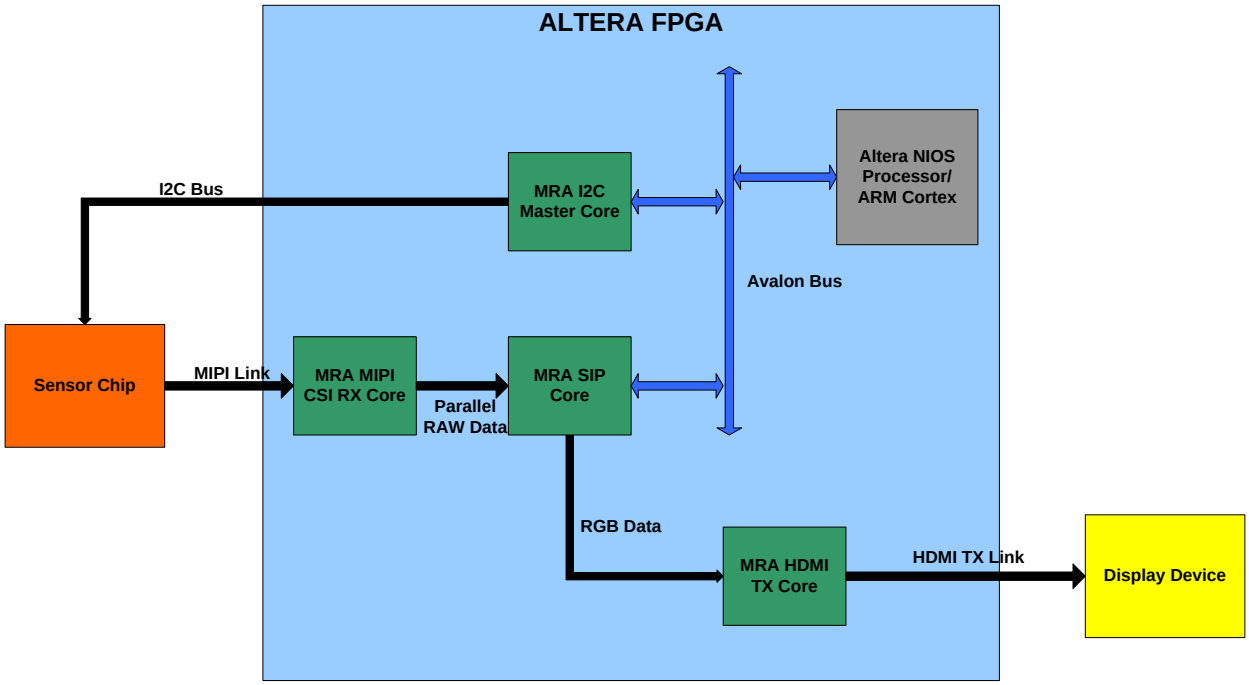

Figure 2: MRA Image Capture Solution

The ISP IP Cores can be used as a complete system or can be re-organized to create a custom solution that meets those critical requirements of your project. MRA Digital offers a comprehensive suite of real-time, low latency video processing cores ranging from Analog Style Digital Zoom, Frame Rate Conversion, Sensor Pipelines and much more.

10.0 Core Functional Description

Figure 1 shows the basic building blocks of the ISP core which include:

- Defective Pixel Correction
- Demosaic
- Black Level Offset
- Image Statistics
- Auto White Balance Correction
- Manual White Balance Correction
- Color Correction
- Saturation Adjustment
- 2D Noise Reduction
- Gamma Corrections

In addition, the following modules can also be added optionally:

- Auto Exposure
- Motion Adaptive Noise Reduction
- RGB to YCbCr Color-Space Conversion
- Frame Buffer

A brief description of the basic building blocks is given below:

Defective Pixel Correction (DPC): The Defective Pixel Correction block performs real-time detection and correction of defective pixels in a camera image sensor array. The core implements a median filter which is used to detect the defected pixel and replace it with median value of the neighboring pixels.

Demosaic: The Demosaic block takes the raw pixel data in Bayer pattern, perform interpolation and reconstruct a full color image in RGB format.

Black Level Offset: This module is used to subtract the color specific offset for each color in order to obtain optimal Black level for each color.

Image Statistics: The Image Statistics block collects various statistics information about the image and updates that information in the memory mapped registers which is then later used to perform Auto Exposure and Auto White Balance correction.

Auto-White Balance (AWB): The AWB block performs Auto White Balance Correction using the Histogram method.

Manual White Balance Correction: The block performs White Balance Correction for some specific condition. Either AWB or Manual correction can be enabled at a given time.

Color Correction: This module is used to perform corrections for each color component which has been introduced due to various spectral characteristics of the optics, light source variations and sensor color filters. The module contains programmable coefficient matrix multipliers with offset compensation that can be used in color correction operations.

Saturation Adjustment: The Saturation Adjustment block adjusts the color saturation of the image.

2D Noise Reduction: The 2D Noise Reduction block performs 2D spatial noise reduction on the image. The 2D noise filter operates on a 5 x 5 filtering window for each color plane.

Gamma Correction (GC): The GC block manipulates image data to match the non-linear response of display devices. The GC implements programmable look-up table structures to implement a gamma correction curve transformation.

For further details about these modules and for the optional modules, please contact MRA.

11.0 Memory Map

The following registers can be used to modify the parameters of each block in the ISP-IP Core. They can be accessed through the Avalon interface. Please contact MRA for further details. Customized registers can also be added based on users specific requests.

Address Offset	Register	Access Type	Bit Width	Bit Offset	Default Value	Description
0	rev_id	R	32	31:0	0x1	Core Revision ID.
4	irq_en	RW	1	0	0x0	Interrupt Enable. Bit 0 : If '1', an interrupt is generated whenever a new frame is detected. Bits 31:1: Reserved.
8	clr_irq	W	1	0	0x0	Write '1' to clear the interrupt. Write-only bit. Always returns '0' if read.
Defect Pixel Correction						

16	dpc_bypass	RW	1	0	0x1	Bypass Defect Pixel Correction Block.
16	dpc_median_threshold	RW	16	31:16	0xFFFF	Median threshold value. If the absolute difference between the current pixel value and the median value of the neighboring 9 pixels is greater than dpc_median_threshold, then the current pixel is replaced by the median value of the 9 neighboring pixels.
Demosaic						
20	demosaic_vert_res	RW	11	10:0	1080	Vertical resolution of the input video.
20	demosaic_bayer_pattern_format	RW	2	13:12	0	Bayer pattern format. Don't touch.
20	demosaic_edge_dup_sel	RW	1	16	1	When '1', it duplicates border columns and rows to perform interpolation at the border. When '0', it adds rows and columns filled with zeroes to perform interpolation at the border.
Black Level Offset Correction						
24	blacklevel_bypass	RW	1	0	1	Bypass Black Level Offset block.
24	blacklevel_red_offset	RW	12	27:16	0	Current Red Pixel - blacklevel_red_offset
28	blacklevel_green_offset	RW	12	11:0	0	Current Green Pixel - blacklevel_green_offset
28	blacklevel_blue_offset	RW	12	27:16	0	Current Blue Pixel - blacklevel_blue_offset
32	blacklevel_underflow	RW	3	2:0	0	Underflow indicator for each color component {R,G,B} after offset correction. Sticky bits. Write '1' on each bit to clear it.
Auto White Balance Correction						
76	awb_corr_bypass	RW	1	0	1	Bypass AWB Histogram block.
80	awb_corr_hist_hismin_red	RW	32	31:0	0	N * (1 – S2/100) Where, $N = 2^{pDATA\_WIDTH} - 1$
84	awb_corr_hist_hismax_red	RW	32	31:0	0	N * S1/100 Where, $N = 2^{pDATA\_WIDTH} - 1$
88	awb_corr_hist_hismin_green	RW	32	31:0	0	N * (1 – S2/100) Where, $N = 2^{pDATA\_WIDTH} - 1$
92	awb_corr_hist_hismax_green	RW	32	31:0	0	N * S1/100

						Where, $N = 2^{pDATA\_WIDTH} - 1$
96	awb_corr_hist_hismin_blue	RW	32	31:0	0	N * (1 – S2/100) Where, $N = 2^{pDATA\_WIDTH} – 1$
100	awb_corr_hist_hismax_blue	RW	32	31:0	0	N * S1/100 Where, $N = 2^{pDATA\_WIDTH} - 1$
104	awb_corr_hist_rdaddr	RW	12	11:0	0	Read Address for a particular location in the Histogram RAM. The 2 MSB bits are always used to select Histogram of the corresponding color. 00: Red 01: Green 10: Blue In order for the read operation to work, the AWB block must be in Capture mode.
104	awb_corr_hist_capture	RW	1	16	0	When set, puts the AWB block in Capture mode. The histogram RAMs aren't updated when Capture mode is enabled. This bit should be '1' during the entire course of read operation i.e. until all the histogram values are read.
104	awb_corr_hist_rdreq	RW	1	20	0	Read Request for the Histogram RAM. Software must set this bit to '1' and also updates awb_corr_hist_rdaddr register to initiate a new Read request.
108	awb_corr_hist_rdone	R	1	0	0	Software must poll this bit after initiating new Read Request. When the read data is available, this bit becomes '1'. This bit automatically clears to '0' when a new Read Request is initiated.
112	awb_corr_hist_rdata	R	32	31:0	0	Histogram Read data addressed by awb_corr_hist_rdaddr register.
116	awb_corr_hist_rsum	R	32	31:0	0	Sum of Red Color components in the last frame.
120	awb_corr_hist_gsum	R	32	31:0	0	Sum of Green Color

						components in the last frame.
124	awb_corr_hist_bsum	R	32	31:0	0	Sum of Blue Color components in the last frame.
Color Correction						
128	colorcorr_bypass	RW	1	0	1	Color Correction Block.
128	colorcorr_coeff_rr	RW	16	31:16	0	RR coefficient for Color Correction matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
132	colorcorr_coeff_rg	RW	16	15:0	0	RG coefficient for Color Correction matrix.. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
132	colorcorr_coeff_rb	RW	16	31:16	0	RB coefficient for Color Correction matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
136	colorcorr_coeff_gr	RW	16	15:0	0	GR coefficient for Color Correction matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
136	colorcorr_coeff_gg	RW	16	31:16	0	GG coefficient for Color Correction matrix.. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0

						represents the magnitude and are **NOT** in 2's complement format.
140	colorcorr_coeff_gb	RW	16	15:0	0	GB coefficient for Color Correction matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
140	colorcorr_coeff_br	RW	16	31:16	0	BR coefficient for Color Correction matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
144	colorcorr_coeff_bg	RW	16	15:0	0	BG coefficient for Color Correction matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
144	colorcorr_coeff_bb	RW	16	31:16	0	BB coefficient for Color Correction matrix.. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
Saturation Adjustment						
192	saturation_bypass	RW	1	0	1	Bypass saturation Adjustment Block.
192	saturation_coeff_rr	RW	16	31:16	0	RR coefficient for saturation adjustment matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the

						magnitude and are **NOT** in 2's complement format.
196	saturation_coeff_rg	RW	16	15:0	0	RG coefficient for saturation adjustment matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
196	saturation_coeff_rb	RW	16	31:16	0	RB coefficient for saturation adjustment matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
200	saturation_coeff_gr	RW	16	15:0	0	GR coefficient for saturation adjustment matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
200	saturation_coeff_gg	RW	16	31:16	0	GG coefficient for saturation adjustment matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
204	saturation_coeff_gb	RW	16	15:0	0	GB coefficient for saturation adjustment matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
204	saturation_coeff_br	RW	16	31:16	0	BR coefficient for saturation adjustment

						matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
208	saturation_coeff_bg	RW	16	15:0	0	BG coefficient for saturation adjustment matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
208	saturation_coeff_bb	RW	16	31:16	0	BB coefficient for saturation adjustment matrix. 16-bit number. Bit 15 is the Sign bit (0 for positive, 1 for negative). Bits 14:12 are integer bits. Bits 11:0 are fractional bits. Bits 14:0 represents the magnitude and are **NOT** in 2's complement format.
Gamma Correction						
960	gamma_bypass	RW	1	0	1	Bypasses Gamma Lookup table.
960	gamma_update	RW	1	4	0	Put the Gamma update tables in update mode. This bit must be set to '1' before updating Gamma Lookup table values. Should be clear to '0', once update operation is completed.
960	gamma_color_id	RW	2	9:8	0	During Gamma update mode or during read operation, these bits select the Lookup table for the given color. 0: Red 1: Green 2: Blue

Table 4: ISP-IP Core Memory Map